UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,372	09/12/2003	Takahiro Imai	81751.0065	6684

26021 7590 04/27/2005

HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/661,372	IMAI, TAKAHIRO	
	Examiner	Art Unit	
	Alonzo Chambliss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *20-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-19* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/12/03*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-19 in the reply filed on 4/4/05 is acknowledged.

2. Claims 20-36 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected product claims, there being no allowable generic or linking claim.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 9/12/03 was filed before the mailing date of the non-final rejection on 4/22/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the

description: 84 in Fig. 13. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the " wherein the second conductive layer has a portion extending in a direction parallel to the semiconductor chips in order to electrically connect the first conductive layers of the semiconductor chips which are irregularly stacked in the step (f); and wherein a part of the second conductive layer is formed on the projecting portion of the insulator must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: " METHOD OF FABRICATING STACKED SEMICONDUCTOR CHIPS ".

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-11, 13, and 19 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Bertin et al. (US 5,571,754).

With respect to Claims 1 and 19, Bertin teaches forming a groove 12 on a first surface of a semiconductor substrate 10 with a plurality of integrated circuits and electrodes (i.e. transfer wirings and electrodes) being formed on the first surface. Forming an insulating layer 14 (i.e. passivation layer) on an inner surface of the groove 12. Forming a first conductive layer 16 or 16' on the insulating layer 14 on the inner surface of the groove 12. Grinding a second surface of the semiconductor substrate 10 opposite to the first surface until the groove 12 is exposed to divide the semiconductor substrate 10 into a plurality of semiconductor chips 11 each of which has a first conductive layer 16' exposed on a side surface of each of the semiconductor chips 11. Stacking the semiconductor chips 11 and electrically connecting the first conductive layer 16' one of the semiconductor chips 11 with the first conductive layer 16' of another one of the semiconductor chips (see col. 5 lines 12-67, col. 1-67; Figs. 1-8 and 12).

With respect to Claims 2 and 3, Bertin teaches wherein the insulating layer is continuously formed from the inner surface of the groove to the first surface in the step (b) and wherein the first conductive layer is continuously formed from the inner surface of the groove to the first surface in the step (c) (see Figs. 2 and 3).

With respect to Claim 4, Bertin teaches wherein the first conductive layer is electrically connected to one of the electrodes in the step (c) (see col. 6 lines 5-15; Figs. 4-6).

With respect to Claim 5, Bertin teaches wherein the semiconductor chips are stacked so that the first surfaces of the semiconductor chips on which the electrodes are formed are oriented to the same direction in the step (e) (see Figs. 7, 8, and 12).

With respect to Claim 6, Bertin teaches wherein the semiconductor chips are stacked so that the first surface of one of the semiconductor chips on which the electrodes are formed is oriented opposite to the first surface of another one of the semiconductor chips on which the electrodes are formed in the step (e) (see Fig. 12).

With respect to Claim 7, Bertin teaches wherein the step (e) includes providing at least one insulator 20 (i.e. passivation layer) between the semiconductor chips (see col. 6 lines 5-15; Figs. 7, 8, and 12).

With respect to Claim 8, Bertin teaches wherein the insulator projects (i.e. the portion of the insulator that extends from side surfaces of the semiconductor chips even with the first conductive layer) in the step (e) (see Fig. 6).

With respect to Claim 9, Bertin teaches wherein the step (f) includes forming a second conductive layer 35, 36, 55, 56, or 100 electrically connects the first conductive layers on a side surface of at least one of the semiconductor chips (see Figs. 7, 8, and 12).

With respect to Claim 10, Bertin teaches wherein the second conductive layer 36 or 56 is extended in a direction perpendicular to the semiconductor chip in order to electrically connect the first conductive layers of the semiconductor chips which are stacked straight in the step (f) (see Figs. 7 and 8).

With respect to Claim 11, Bertin teaches wherein the second conductive layer 35 or 55 has a portion extending in a direction parallel to the semiconductor chips in order to electrically connect the first conductive layers of the semiconductor chips which are irregularly stacked in the step (f) (see Figs. 7 and 8).

With respect to Claim 13, Bertin teaches wherein the second conductive layer (i.e. the solder bump in combination with metallization 100) is formed of a solder in the step (f) (see col. 7 lines 50-67).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al. (US 5,571,754) as applied to claim 1 above, and further in view of Senba et al. (US 5,973,392) and Fukunaga et al. (US 6,730,596).

With respect to Claim 14, it is well known in the semiconductor industry to formed a conductive layer by supplying a solvent containing particles in the step (f) as evident by Fukunaga (see col. 3 lines 60-67 and col. 4 lines 46-59).

With respect to Claims 15 and 18, Bertin fails to disclose mounting the semiconductor chips on a substrate and electrically connecting the semiconductor chips to an interconnecting pattern of the substrate. However, Senba discloses mounting the semiconductor chips 1 on a substrate 8 and electrically connecting the semiconductor chips 1 to an interconnecting pattern of the substrate 8 (see col. 4 lines 22-54; Figs. 3C, and 4C). It is well known in the semiconductor industry to form a conductive layer by supplying a solvent containing particles in the step (f) as evident by Fukunaga (see col.

3 lines 60-67 and col. 4 lines 46-59). Thus, Bertin and Senba have substantially the same environment of semiconductor chips stack on top of each other with the solder bumps attached to the lower surface of first chip. Therefore, it would have been obvious to one skilled in the art at the time of the invention to attached a mother board to the solder bumps of Bertin, since the mother board provides a reliable support for the semiconductor chips while electrically connecting other device on the mother board to the semiconductor chips as taught by Senba.

With respect to Claim 16, the combination of Bertin-Senba inherently discloses wherein the steps (e) and (g) are performed before the steps (f) and (h).

With respect to Claim 17, Senba discloses wherein a solder is used to electrically connect the first conductive layers to the interconnecting pattern in the step (h) (see Figs. 3C, 4C, and 5B).

Allowable Subject Matter

12. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowance subject matter: the prior art of record does not teach or suggest the combination of wherein the second conductive layer has a portion extending in a direction parallel to the semiconductor chips in order to electrically connect the first conductive layers of the semiconductor chips which are irregularly stacked in the step (f); and wherein a part of

the second conductive layer is formed on the projecting portion of the insulator in claim 12.

The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

Conclusion

13. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.

Alonzo Chambliss
Primary Patent Examiner
Art Unit 2814

AC/April 22, 2005